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(71) Applicant: FUJITSU LIMITED
1015, Kamikodanaka Nakahara-ku
Kawasaki-shi Kanagawa 211 (JP)

(72) Inventor: Tanikawa, Akinao
1075-10, Ichigao Midori-ku
Yokohama-shi Kanagawa 227 (JP)

Ohshima, Toshiharu
997-2, Chitose Takatsu-ku
Kawasaki-shi Kanagawa 213 (JP)

Sakai, Toshihiro
231-22, Hiyoshihon-cho§Kohoku-ku
Yokohama-shi Kanagawa 223 (JP)

(74) Representative: Billington, Lawrence Emlyn et al
HASELTINE LAKE & CO Hazlitt House 28 Southampton
Buildings Chancery Lane
London WC2A 1AT (GB)

(54) Direct memory access controlled system.

(57) A direct memory access (DMA) controlled system which performs DMA data transfer between a main memory (21), a cache memory (7), and disk memories (5,6) while exchanging DMA transfer requests and acknowledgements among disk control units (2,3), a memory-to-memory transfer control unit (13), and a common DMA control unit (12). The data transfer speed between the main memory (21) and cache memory (7) is variable according to the load condition of the DMA control unit (12) for the disk memories (5,6), enabling the transfer capability of the DMA control unit (12) to be kept at a fixed, continually high level.

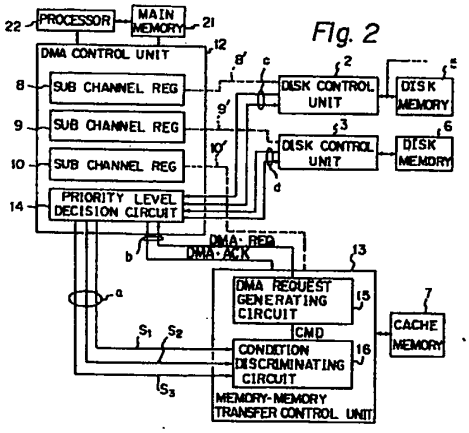

Fig. 2

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Description

DIRECT MEMORY ACCESS CONTROLLED SYSTEM

The present invention relates to a system controlled by a direct memory access (hereinafter referred to as DMA) method.

For example, a DMA control unit is used in a computer system to reduce the load of a central processing unit (CPU) by transferring data between a main memory and sub memory and transferring data between a sub memory and auxiliary memory. The "main memory" refers to the system memory which performs data communication with the CPU and is also called the main storage. The "sub memory" is the memory which performs data communication with the main memory and, for example, corresponds to a so-called cache memory. Further, the "auxiliary memory" is an external memory which, for example, corresponds to a disk memory. Usually, a plurality of disk memories are provided. Disk memories, i.e., auxiliary memories, are connected to the DMA control unit through auxiliary memory control units, i.e., disk control units, provided corresponding to the same. Similarly, the cache memory is connected to the DMA control unit through a memory-to-memory transfer control unit. In this case, the total of the sum (CP_{dk}) of the data transfer capabilities of the respective disk control units and the data transfer capability (CP_{mm}) of the memory-to-memory transfer control unit ($CP_{dk} + CP_{mm}$) must be smaller than the data transfer capability (CP_{dma}) of the DMA control unit, i.e., $CP_{dk} + CP_{mm} \leq CP_{dma}$. If the inequality symbol (<) becomes opposite, the DMA control unit would become inoperative due to insufficient capability. In this case, it would be possible to increase the data transfer capability of the DMA control unit to make up for the insufficient capability, but this would require an increase of the hardware amount of the DMA control unit and would not be advantageous from an economic viewpoint.

As described later in detail, in previously proposed DMA control units, a status of the sub channel (control information of each of the above DMA control units) is not known. Therefore, even when the number of data transfer requests becomes maximum, a certain restriction is applied so that the data transfer capability (CP_{dma}) of the DMA control unit is not exceeded. This restriction means that the data transfer capability of the memory-to-memory transfer control unit is always kept at a constant level (for example, 1 Mbyte).

Therefore, when one of two disk control units does not issue a data transfer request to the DMA control unit, that is, when there is a margin in the capability of the DMA control unit, despite it being possible to increase the data transfer capability of the memory-to-memory control unit by an amount corresponding to the margin, the data transfer capability of the memory-to-memory transfer control unit remains restricted to the set level (for example, 1 Mbyte). Therefore, in previous DMA control systems, there is the disadvantage of a deteriorated data transfer efficiency.

The present invention addresses the problem of providing a DMA controlled system where the data transfer efficiency under a DMA mode is improved to the theoretically maximum attainable level.

According to the present invention there is provided a DMA (direct memory access) controlled system including a main memory, a sub memory and one or more auxiliary memories;

a memory-to-memory transfer control unit for controlling data transfer between said main memory and sub memory, operable under a variable data transfer speed;

one or more auxiliary control units for controlling data transfer between said sub memory and auxiliary memories, operable under a constant data transfer speed; and

a DMA control unit operable to cooperate with said memory-to-memory transfer control unit and said auxiliary control units to control direct memory access (DMA) data transfer;

wherein said DMA control unit employs therein priority level decision means for providing condition signals indicating the operational state of the auxiliary memories according to status of a sub channel determined by said auxiliary control units; and

said memory-to-memory transfer control unit employs therein condition discriminating means for determining a data transfer speed of said memory-to-memory transfer control unit according to said condition signals and DMA request generating means for enabling to make variable a time interval for issuing DMA request signals to be output to said DMA control unit according to various speed specifying commands issued from said condition discriminating means;

whereby when said auxiliary control units are busy and a margin of data transfer capability of said DMA control unit decreases, the data transfer speed of said memory-to-memory transfer control unit is suppressed so as to conform with said decreased margin.

The inventors of the present invention have made use of the following idea. When there is a margin in the data processing capability of a DMA control unit, the data transfer speed between a sub memory and main memory may be made faster. Conversely, when there is no margin in the data processing capability of a DMA control unit, it may be made slower. Taking note of this, the memory-to-memory transfer control unit may be constructed so the memory-to-memory data transfer speed is automatically changeable in accordance with the load condition of the DMA control unit.

Reference is made, by way of example, to the accompanying drawings, in which:

Fig.1 is a block diagram showing the schematic construction of a previously proposed DMA controlled system;

Fig.2 is a block diagram showing the principle of a DMA controlled system of the present invention;

Fig.3 is a block diagram showing an example of the memory-to-memory transfer control unit for use in the present invention;

Fig.4 is a view showing an example of a discrimination logic of a discriminator of Fig.3;

Fig.5 is a block diagram showing a detailed example of a DMA controlled system to which the present invention is applied;

Fig.6 is a circuit diagram showing a specific example of a DMA control unit;

Fig.7 is a block diagram showing a specific example of a priority level decision circuit;

Fig.8 is a circuit diagram showing a specific example of a condition discriminating circuit;

Fig.9 is a circuit diagram showing a specific example of a DMA request generating circuit; and

Fig.10 is a block diagram showing a specific example of a disk control unit.

To facilitate understanding of the present invention, before explaining the construction of the present invention, mention will be made of a previously proposed DMA control system.

Figure 1 is a block diagram showing a schematic construction of a proposed DMA control system. In Fig. 1, the DMA control unit 1 is connected to and operates with auxiliary control units, i.e., disk control units 2 and 3 and also the memory-to-memory transfer control unit 4. The disk control units 2 and 3 have cooperating with them respectively at least one auxiliary memory, i.e., disk memory. Further, the memory-to-memory transfer control unit 4 has cooperating with it a sub memory, i.e., cache memory 7.

The disk control units 2 and 3 and the memory-to-memory transfer control unit 4 issue to a priority level decision circuit 11 in the DMA control unit 1 a signal for requesting to the DMA control unit 1 data transfer control, i.e., a DMA request signal DMA REQ. When acknowledgement of this request, i.e., a DMA acknowledge signal DMA ACK, is received, the disk control unit 2 cooperates with a sub channel register (REG) 8 (shown schematically by broken line 8') to execute the data transfer. Similarly, the disk control unit 3 cooperates with a sub channel register (REG) 9 (9') and the memory-to-memory transfer control unit 4 cooperates with a sub channel register (REG) 10 (10') to execute the respective data transfers. In this case, if, for example, the data transfer capability of the DMA control unit 1 is 6 Mbyte, the data transfer capability of the disk control units 2 and 3 is respectively 2.5 Mbyte, and the data transfer capability of the memory-to-memory transfer control unit 4 is a maximum 2.5 Mbyte, the total of the data transfer capability of the control units 2, 3, and 4, i.e., 7.5 Mbyte, would exceed the data processing capability (6 Mbyte) of the DMA control unit 1.

To prevent this overload from occurring, previously the data transfer capability of the memory-to-memory transfer control unit 4 has been fixed to a certain level (according to the above example, 1 (= 6 - 2.5 × 2) Mbyte). This may be achieved by hardware or software.

However, as mentioned earlier, if the data transfer capability of the memory-to-memory transfer control unit 4 is fixed to a certain level at all times, the data transfer efficiency of the DMA controlled system deteriorates and, as a result, the data processing speed of the system is reduced.

Next, an explanation will be made of a DMA controlled system embodying the present invention.

Figure 2 is a block diagram showing the principle of the DMA controlled system . To make the explanation easier to understand, we assume the data transfer capabilities to be as follows, for example:

DMA control unit 12: 6 Mbyte
Disk control unit 2: 2.5 Mbyte
Disk control unit 3: 2.5 Mbyte
Memory-to-memory transfer control unit 13: Max. 4 Mbyte

Here, we assume the disk control units 2 and 3 and the memory-to-memory transfer control unit 13 have issued a DMA request signal to the priority level decision circuit 14 of the DMA control unit 12. The priority level decision circuit 14 accepts the DMA request from the unit with the highest priority (in this case, we assume the priority of the disk control units 2 and 3 is higher than the priority of the memory-to-memory transfer control unit 13) and applies a DMA start signal S_1 to a condition discriminating circuit 16 in the memory-to-memory transfer control unit 13. Soon after this, the condition discriminating circuit 16 returns a DMA acknowledge (ACK) signal DMA ACK to the disk control units 2 and 3 during the transfer of data.

Further, the priority level decision circuit 14 applies control information of the sub channel registers 8 and 9 upon application of the DMA start signal and a memory identification (ID) signal S_2 during the execution of the data transfer to the condition discriminating circuit 16. When the afore-mentioned DMA acknowledge signal (DMA ACK) is received, it is determined from the ID signal S2 that the disk control unit 2 or 3 has begun the data transfer and a command is issued to the DMA request generating circuit 15 to reduce the data transfer speed.

The DMA request generating circuit 15 elongates the interval for issuing the DMA request signal (DMA REQ) to be given to the priority level decision circuit 14 to adjust the data transfer speed to 1 Mbyte (1 + 2.5 × 2 = 6). That is, low speed data transfer is performed.

When the data transfer based on the control information of the sub channel register 8 or 9 is finished, the priority level decision circuit 14 applies a DMA transfer stop signal S_3 to the condition discriminating circuit 16 and makes notification of the control unit (2, 3) for which data transfer has finished by the ID signal S_2. The condition discriminating circuit 16 can notify which control unit has finished the DMA operation.

By the notification of the completion of the DMA operation, the condition discriminating circuit 16 issues a command to the DMA request generating circuit 15 to raise the data transfer speed. The DMA request

generating circuit 15 shortens the time interval for issuing the DMA request signal (DMA REQ) to be given to the priority level decision circuit 14 and adjusts the data transfer speed to 3.5 Mbyte (3.5 + 2.5 = 6).

Furthermore, the condition discriminating circuit 16 will not give a command to lower the data transfer speed to the DMA request generating circuit when not transferring data under the control of both the sub channel registers 8 and 9, so the memory-to-memory transfer control unit 13 maintains a high data transfer speed of 4 Mbyte. If the control unit (2 or 3) corresponding to the sub channel register 8 or 9 begins data transfer and thus the priority level decision circuit 14 provides a DMA start signal S_1 and ID signal S_2 , the condition discriminating circuit 16 elongates the time interval for issuing the DMA request signal to the DMA request generating circuit 15 so that the data transfer speed becomes 3.5 Mbyte. If both the control units (2 and 3) corresponding to the sub channel registers 8 and 9 are transferring data, the time interval is adjusted so that data transfer speed of the memory-to-memory transfer control unit 13 becomes 1 Mbyte.

Due to the above construction, the condition discriminating circuit 16 can determine the operational state of the sub channel registers 8 and 9 by supervising the signals S_1 and S_2 provided from the priority level decision circuit 14 and, in accordance with the operational state, can elongate or shorten the time interval for issuing a DMA request DMA REQ for the DMA request generating circuit 15. Therefore, the memory-to-memory transfer control unit 13 can perform automatic control to achieve the maximum data transfer capability of the DMA control unit 12. As a result, a DMA controlled system able to perform high efficiency data processing can be realized.

Figure 3 is a block diagram showing an example of a memory-to-memory transfer control unit according to the present invention. In Fig. 3, the memory-to-memory transfer control unit 13 comprises, as shown in Fig. 2, a DMA request generating circuit 15 and a condition discriminating circuit 16. First, the condition signals provided from the priority level decision circuit 14 (Fig. 2), i.e., the DMA start signal S_1 , ID signal S_2 , and DMA transfer stop signal S_3 , are input to a decoder 17 and decoded to produce, for example, three types of decoded output signals S_4 , S_5 , and S_6. These signals S_4 , S_5 , and S_6 are input to a discriminator 18. The decoder 17 and discriminator 18 comprise the condition discriminating circuit 16.

Figure 4 is a view showing an example of a discrimination logic of the discriminator of Fig. 3. An explanation will be made of the operation of Fig. 3 with reference to this discrimination logic. If S_4 = "0", S_5 = "0", and S_6 = "1", the discriminator 18 issues a command CMD to the effect that the data transfer speed should be made high speed (HIGH).

The command CMD is input to a counter 19 and the output of the counter 19 controls a DMA request generator 20. The counter 19 and generator 20 comprise the DMA request generating circuit 15.

When the discriminator 18 issues a high speed command, the counter 19 counts a lower number corresponding to the high speed command and, when it finishes, controls the DMA request generator 20 to output to the unit 12 a DMA request signal DMA REQ.

If the output signals of the decoder 17 are S_4 = "1", S_5 = "0", and S_6 = "1", the discriminator 18 issues a command CMD to the effect that the data transfer speed should be made middle speed (MID). Similarly when S_4 = "0", S_5 = "1", and S_6 = "1", the discriminator 18 issues a middle command CMD. At this time, the counter 19 counts a number corresponding to the middle speed command and, when it finishes, controls the DMA request generator 20 to output to the unit 12 a DMA request signal DMA REQ.

If the output signals of the decoder 17 and S_4 = "1", S_5 = "1", and S_6 = "1", the discriminator 18 issues a command CMD to the effect that the data transfer speed should be made low speed (LOW). At this time, the counter 19 counts a larger number corresponding to the low speed command and, when it finishes, controls the DMA request generator 20 to output to the unit 12 a DMA request signal DMA REQ.

Note that when the signal S_6 is S_6 = "0", this means no data transfer is being performed between the memory-to-memory transfer control unit 13 and the cache memory, so the discriminator 18 does not issue any command CMD to the counter 19 regardless of the "1" or "0" state of S_4 and S_5. This is because there is no need to output a DMA request signal from the memory-to-memory transfer control unit 13.

Figure 5 is a block diagram showing a detailed example of a DMA controlled system to which the present invention is applied. Note that throughout the figures, the same constituent elements are given the same reference numerals or symbols. In the figure, the link a and links b, b′ connecting the DMA control unit 12 and memory-to-memory transfer control unit 13 are particular characteristics of the present invention. The link a is shown in Fig. 2 as well and is used for transmission of control signals S_1 , S_2 , and S_3. The link b is shown in Fig. 2 as well, but in actuality, the link b′ is also used. The links c and d connect to the disk control units 2 and 3. In addition, reference numeral 21 indicates the already mentioned main memory, and 22A and 22B processors. The two processors share roles and are formed by a combined processor in a high speed computer system. Reference numerals 23 and 24 are bus arbiters which designate the opening or closing of the two-way gates 25 and order traffic so that there is no conflict in data transmission on the memory bus 26 and input/output (I/O) bus 27.

The processor 22 operates as if to directly access the disk memories 5 and 6, but in the system of Fig. 5, the cache memory 7 has copied and stored therein the desired data in the disk memories 5 and 6 and the cache memory 7 is accessed, wherein the processor 22 can process data much faster. Note that in general a disk cache memory is provided as part of the disk memories 5 and 6, but this makes it impossible to use generalpurpose disk memories, so is disadvantageous economically. A concern of the present invention is to make the DMA transfer speed between the main memory 21 and the cache memory 7 in Fig. 5 variable.

First, when the DMA mode starts, the processor 22 writes the DMA control information in the corresponding

sub channel registers (8, 9, 10, 10b; 10b relating to the previously mentioned link b') in the DMA control unit 12. At this time, the bus arbiter 24 supervises the address of the I/O bus 27 and if it is the address for the DMA control unit 12 or the disk control unit 2 or 3, drives the receiver side of the two-way gate 25.

Next, the processor 22 writes the address in the disk sector register (shown by 111 in Fig. 10) in the disk control unit 2 or 3. This address indicates the position of the desired data in the disk memory.

The processor 22 displays the DMA start flag (register 112 in Fig. 10) in the disk control unit 2 or 3.

The disk control unit 2 or 3 outputs to the DMA control unit 12 a DMA request signal DMA REQ (Fig. 2).

The disk control unit 2 or 3 sends to the bus arbiter 24 a signal requesting the use of the I/O bus 27.

When a response to the afore-mentioned DMA REQ, i e., a DMA acknowledge signal DMA ACK, is returned from the DMA control unit 12, data begins to be read by the said disk memory. Further, data is transferred from the disk control unit 2 or 3 to the DMA control unit 12.

The DMA control unit 12 sends to the bus arbiter 23 a signal requesting use of the memory bus 26'. When a response to the request for use is returned, the DMA control unit 12 writes data in the cache memory 7.

Further, the DMA control unit 12 outputs a request for use of the memory bus 26 to the bus arbiter 23 and transfers data from the cache memory 7 to the main memory 21 under the control of the memory-to-memory transfer control unit 13. A concern of the present invention is how to issue the DMA request under the control of the memory-to-memory transfer control unit 13.

Figure 6 is a circuit diagram showing a specific example of the DMA control unit. In the figure, the sub channel register 31 comprises all together #0 to #2 registers (corresponding to 8, 9, and 10 in Fig. 2) and a #3 register (register 10b forming a pair with sub channel register 10). More specifically, it is comprised of DMA mode registers (DMR), address registers (ADR) 33, and byte counters (BC) 34. The DMR's 32 have written in them the DMA direction, the first transferred byte number, and the DMA start flag from the processor 22 through the I/O bus 27. The ADR's 33 have written in them the address of the memory bus 26 or 26' from the processor 22. Further, the BC's 34 have displayed therein the number of remaining transfer bytes. A subtractor 35 is provided for displaying the remainder, which subtractor 35 subtracts with each transfer the number of transferred bytes recorded in the DMR 32 (in the figure, shown by -x). When the subtraction finally brings the content of BC to zero, the transfer stops and the signal of stop #0 to #3 is applied to the priority. level decision circuit.

The address register (ADR) 33 designates the head address of the data for which transfer is next to begin with each end of a transfer. For this, an adder 36 is provided, which adds the number of transferred bytes recorded in the DMR 32 (in the figure, indicated by +y).

The above-mentioned sub channel register #3 (corresponding to 10b) in actuality is required for storage in a buffer memory (not shown) in the memory-to-memory transfer control unit 13 (Fig. 5) of data transferred from the cache memory 7 to the main memory 21 for the purpose of error correction. Note that an error correction circuit for the above-mentioned error correction is shown in Fig. 6 as ECC 37.

Figure 7 is a block diagram showing a specific example of a priority level decision circuit and is a more detailed view of the block 14 in Fig. 6. The priority level decision circuit 14, as shown, is comprised of a priority level decision logic 41, response control circuit 42, decoding circuit 43, and OR gate 44. The priority level decision logic 41 receives a DMA request signal DMA REQ from the previously mentioned links c, d, b, and b' and receives on a priority basis the request of the predetermined highest priority. Note that the logic for determination of the priority is known and will not be explained in detail.

For example, when the logic 41 receives a DMA request from the link c, the signal is applied through the line p to the response control circuit 42, the circuit 42 is driven, and an acknowledge signal ACK is generated. Which link the ACK is returned is designated by the line q. On the line q, the ID of the received link, i.e., "c", appears. Based on this "c", the circuit 42 returns ACK to the link c. By this, the disk control unit 2 (Fig. 5) starts DMA transfer of the read data from the disk memory. That is, the circuit 42 applies a DMA start signal to the sub channel register 31 on the one hand, while, on the other hand, the DMA start signal is provided as the control signal S_1 to the condition discriminating circuit 16 (Figs. 2 and 3) in the memory-to-memory transfer control unit 13. The circuit 13 is also provided with a control signal S_2 showing the above-mentioned ID.

When the apparatus which has already executed the DMA transfer, for example, the disk control unit 3 (Fig. 5), finishes the transfer of the predetermined data, a stop #1 signal is sent from the subtractor 35 (Fig. 6) to the priority level decision circuit 14. This stop #1 is received by the decoding circuit 43, whereupon which apparatus the DMA stop signal is from is decoded. In this case, the ID of the DMA stop signal shows the link d, that is, the disk control unit 3. This ID, i.e., "d", is provided to the above-mentioned condition discriminating circuit 16 in the memory-to-memory transfer control unit 13 through the OR gate as ID signal S_2.

Figure 8 is a circuit diagram showing a specific example of a condition discriminating circuit. This condition discriminating circuit 16, as explained with respect to Fig. 3, may be broken down into a decoder 17 and discriminator 18. Further, S_1, S_2, and S_3, S_4, S_5, and S_6, and command CMD appear in the apparatus shown in Fig. 8.

The ID signal discriminates between the sub channel registers #0 to #3 and can discriminate between them by 2 bits (DI0, DI1). That is, see the following Table I.

Table I

DI0	DI1	Sub channel (31)	Link
0	0	#0	c
0	1	#1	d
1	0	#2	b
1	1	#3	b'

Receiving the ID signals (ID0 and ID1) are the D flip-flops (D FF) 51 to 54. The outputs of D FF 51 and 52 show the ID when a DMA start is issued (START ID0, START ID1), while the outputs of D FF 53 and 54 indicate the ID when a DMA stop is issued (STOP ID0, STOP ID1).

These signals START ID0, ID1 and STOP ID0, ID1 are input to the AND gates 61 to 68 of the next stage. The inputs of the AND gates 61 to 64 are provided with inverters in differing combinations. The AND outputs for which sub channel (#0 to #3) the DMA has started (START 0 to START 3). On the other hand, the inputs of the AND gates 65 to 68 are provided with inverters in differing combinations, and the AND outputs indicate for which sub channel (#0 to #3) the DMA has stopped (STOP 0 to STOP 3).

These signals START 0 to START 3 and STOP 0 to STOP 3 are input to the JK flip-flop (JK FF) of the next stage. The JK FF's have an FF output of "1" when the J-input is "1" and are reset when the K-input becomes "1". Therefore, the outputs of the JK FF's 71 to 74 become signals BSY0 to BSY3 which show which sub channel is busy. The signals BSY0 to BSY3 form the previously mentioned decoded output signals S_4, S_5, and S_6. Note that the signal S_6 is the OR'ed version of BSY2 and BSY3 and therefore an OR gate OR1 is provided. This is because BSY2 and BSY3 never simultaneously become "1".

The signals S_4 to S_6 are input to the AND gates 81 to 84 in the discriminator 18. The inputs of the AND gates 81 to 84 are provided with inverters in differing combinations. The discrimination shown in Fig. 4 is achieved by a simple logic. Note that the OR gate in Fig. 4 (outputting the MID speed command) corresponds to the OR gate OR2 in Fig. 8. Therefore, the high speed command HIGH, middle speed command MID, and low speed command LOW are issued and applied to the counter (19 in Fig. 3). Note that two different types of middle speed commands, such as MID1 and MID2, may be issued from the outputs of the AND gates 82 and 83. The following Table II shows an example of the correspondence between the logic pattern of the busy signals BSY0 to BSY3 and the speed command (CMD).

Table II

BSY 0	BSY 1	BSY 2		BSY 3	CMD	
0	1	2		3		
0	0	0	or	1	HIGH	
		1		0		
0	1	0	or	1	MID1	MID
		1		0		
1	0	0	or	1	MID2	MID
		1		0		
1	1	0	or	1	LOW	
		1		0		

Figure 9 is a circuit diagram showing a specific example of a DMA request generating circuit. This DMA request generating circuit 15 may be largely broken down into a counter 19 and DMA request generator 20 as explained in Fig. 3. It takes as input the speed command CMD shown in Fig. 3 (also shown in Fig. 4 and Fig. 8) and outputs a DMA request signal DMA REQ corresponding to the command.

The counter 19 has as its heart a counting unit 95, which counting unit 95 functions as a down counter from a

subtractor 96. The down counter has a count number initially preset and is supplied with preset numbers from first, second, and third presetters 91, 92, and 93, e.g., so-called dip switches. The presetters 91, 92, and 93 supply small, middle, and large preset numbers respectively. Which preset number is selected is determined in accordance with which of the high, middle, and low speed commands (CMD) is issued. The selection is performed by a selector (SEL) 94.

Whether or not the count of the counting unit 95 has become zero is detected by a zero comparator 97. If not zero (NO), the count operation is continued. When zero is reached (YES), a trigger signal St is issued and output to the DMA request generating circuit 20, simultaneous with which the selector 94 is cleared. Note that the trigger signal St may be obtained via a differentiating circuit (D) 98. The circuit 98 is necessary since the correct DMA request signal cannot be generated if the output of the zero comparator 97 continues forever to be applied to the circuit 20 of the next stage.

The afore-mentioned trigger signal St is input to a DMA request flag flip-flop (REQ FLG FF) 101 and sets the DMA request flag. The DMA request flag is only set at time intervals corresponding to the afore-mentioned speed commands (HIGH, MID, and LOW). When the flag is set, a DMA request signal DMA REQ #2 or DMA REQ #3 is sent via an AND means 102 and SR flip-flop (S/R) 103 to the priority level decision circuit 14 in the DMA control unit 12 (Figs. 2, 6, and 7). When the circuit 14 receives the DMA request, DMA ACK #2 or DMA ACK #3 is returned, whereby the DMA request flag is reset and the next coming new DMA request can be received.

If the memory bus 26 is in a non-use stage, DMA transfer cannot be executed, so it is necessary to check if the memory bus 26 is idle. Therefore, the AND means 101 is provided. The AND means 101 opens when a bus idle signal BSY is received from the bus arbiter 23 and applies the DMA request flag to the SR FF 103. Note that the AND means 101 can be realized by software or hardware.

The DMA REQ #2 and DMA REQ #3 correspond to the DMA data transfer to the cache memory 7 and the DMA data transfer from the memory-to-memory transfer control unit 13 (Fig. 5) and correspond to the afore-mentioned sub channel registers #2 and #3. Therefore, the DMA REQ #2 and #3 must be prohibited from existing simultaneously. For this, the SR FF 103 is provided so that DMA REQ #2 and #3 are output complementarily from the set side and reset side.

Figure 10 is a block diagram showing a specific example of a disk control unit. The disk control units 2 and 3 are constructed identically. The disk sector register 111 in the figure has already been explained with reference to Fig. 5. The disk sector register 111 stores the address which determines from which disk memory 5 or 6 to read and cooperates with the disk interface controller 116 as well. The controller 116 is connected to the data buffer 115. When the I/O bus 27 is busy and data read from the disk memory cannot be fed to the bus, the data is stored temporarily in the buffer 115. Whether or not the I/O bus 27 is busy or idle is found from the interrelation with the bus arbiter 24. For this, a bus request controller 113 is provided.

When a request for data transfer is issued in the form of DMA REQ to the priority level decision circuit in the DMA control unit 12 and DMA ACK is returned, the DMA transfer starts. In this case, a command to start the DMA transfer is first set from the processor 22 through the I/O bus 27 in the DMA start flag register 112. By this setting, the bus request controller 113 confirms the occupancy of the I/O bus. If occupancy is possible, the afore-mentioned DMA REQ is issued.

As mentioned above, in embodiments of the present invention, the DMA data transfer between the main memory and sub memory, i.e., cache memory, is made variable in speed. Further, the transfer speed is made selectable in accordance with the load state of the other auxiliary memories of the DMA control unit, i.e., the disk memories. Therefore, the DMA controlled system is given an overall improved data transfer efficiency.

Claims

1. A DMA (direct memory access) controlled system including a main memory, a sub memory and one or more auxiliary memories;

a memory-to-memory transfer control unit for controlling data transfer between said main memory and sub memory, operable under a variable data transfer speed;

one or more auxiliary control units for controlling data transfer between said sub memory and auxiliary memories, operable under a constant data transfer speed; and

a DMA control unit operable to cooperate with said memory-to-memory transfer control unit and said auxiliary control units to control direct memory access (DMA) data transfer;

wherein said DMA control unit employs therein priority level decision means for providing condition signals indicating the operational state of the auxiliary memories according to status of a sub channel determined by said auxiliary control units; and

said memory-to-memory transfer control unit employs therein condition discriminating means for determining a data transfer speed of said memory-tomemory transfer control unit according to said condition signals and DMA request generating means for enabling to make variable a time interval for issuing DMA request signals to be output to said DMA control unit according to various speed specifying commands issued from said condition discriminating means;

whereby when said auxiliary control units are busy and a margin of data transfer capability of said DMA

control unit decreases, the data transfer speed of said memory-to-memory transfer control unit is suppressed so as to conform with said decreased margin.

2. A system according to claim 1, wherein said sub memory is a cache memory and said the or each auxiliary memory is a disk memory.

3. A system according to claim 1 or 2, wherein said priority level decision means provides at least three types of condition signals, a first one being a DMA start signal, a second one an identification (ID) signal, and a third one a DMA stop signal, said ID signal indicating a number of a sub channel register for which DMA has started or a number of a sub channel register for which DMA has stopped.

4. A system according to claim 3, wherein said condition discriminating means comprises a decoder which receives as input said DMA start signal, ID signal, and DMA stop signal and produces decoded output signals consisting of a plurality of bits and a discriminator which receives as input the pattern of the plurality of bits from said decoder and selects a corresponding one of at least a high speed command, middle speed command, and low speed command.

5. A system according to claim 4, wherein said DMA request generating means comprises a counter which counts a large, middle, and small (including zero) count number according to one of said high speed, middle speed, and low speed commands and a DMA request generator which outputs to said DMA control unit a DMA request signal having a small, middle, and large time interval according to said small, middle, and large count number, respectively.

6. A system according to claim 3, 4, or 5, wherein said priority level decision means comprises:

a priority level decision logic which receives DMA request signals, selects the request with the high priority, and outputs said identification (ID) signal for discriminating the selected memory and outputs a receipt signal showing the receipt of the request;

a response control circuit which, when said receipt signal and identification signal are received, returns a DMA acknowledge signal to the memory control unit which issued said DMA request and further issues said DMA start signal;

a decoding circuit which, when the memory control unit which issued said DMA request finishes the DMA data transfer, issues said DMA stop signal and further outputs an identification (ID) signal discriminating the memory control unit; and

an OR gate for OR'ing an identification (ID) signal of said DMA start signal output and identification (ID) signal of said DMA stop signal output.

7. A system according to claim 6, wherein a sub channel register which receives at least said DMA start signal and identification (ID) signal to form control. information is provided in the DMA control unit, said sub channel register applying a detection signal to said decoding circuit when completion of each DMA data transfer is detected and causing to be output said identification (ID) signal from said decoding circuit.

8. A system according to claim 4 or 5, or claim 6 or 7 as appended to claim 4, wherein said decoder comprises:

two start side D flip-flops which receive commonly at each D-input said DMA start signal and which receive separately an identification (ID) signal of two bits;

two stop side D flip-flops which receive commonly at each D-input said DMA stop signal and which receive separately an identification (ID) signal of two bits;

start side AND gates which judge from the combination of the bits of the outputs of said two start side D flip-flop which memory control unit the DMA start signal is from;

stop side AND gates which judge from the combination of the bits of the outputs of said two stop side D flip-flops which memory control unit the DMA stop signal is from; and

JK flip-flops which receive as J-inputs the outputs from said start side AND gates and receive as K-inputs the outputs from said stop side AND gates, the outputs of said JK flip-flops being used as said decoded output signals.

9. A system according to claim 8, wherein said discriminator is comprised of AND gates which receive as inputs said decoded output signals and open only when said bit pattern is matched, said AND gates being at least three AND gates which output said high speed, middle speed, and low speed commands.

10. A system according to claim 5, or any one of claims 6 to 9 as appended to claim 5, wherein said counter comprises:

presetters which supply said large, middle, and small count numbers to be preset to said counting unit;

a selector which selects one of the outputs of said presetters according to one of said high, middle, and low speed commands for presetting said counting unit;

a zero comparator which detects whether the count number of said counting unit has reached zero and continues said down count until zero is reached; and

a differentiating circuit which differentiates said zero comparator output to generate a trigger signal when said count number reaches zero.

11. A system according to claim 10, wherein said DMA request generator comprises:

a flag flip-flop which receives said trigger signal to set a DMA request flag;

AND means which confirms that the memory bus on which data transfer is to be made based on said DMA request is not being used and then passes said DMA request signal; and

an RS flip-flop which complementarily sends to said priority level decision circuit two DMA request signals according to the DMA request signal passing through said AND means;

said two DMA request signals indicating data transfer from said cache memory and data transfer to the cache memory;

said flag flip-flop being reset by each DMA acknowledge signal returned from said priority level decision circuit in response to each said DMA request signal.

12. A system according to claim 11, wherein said AND means notifies whether said memory bus is not being used by a bus arbiter.

Fig. 1

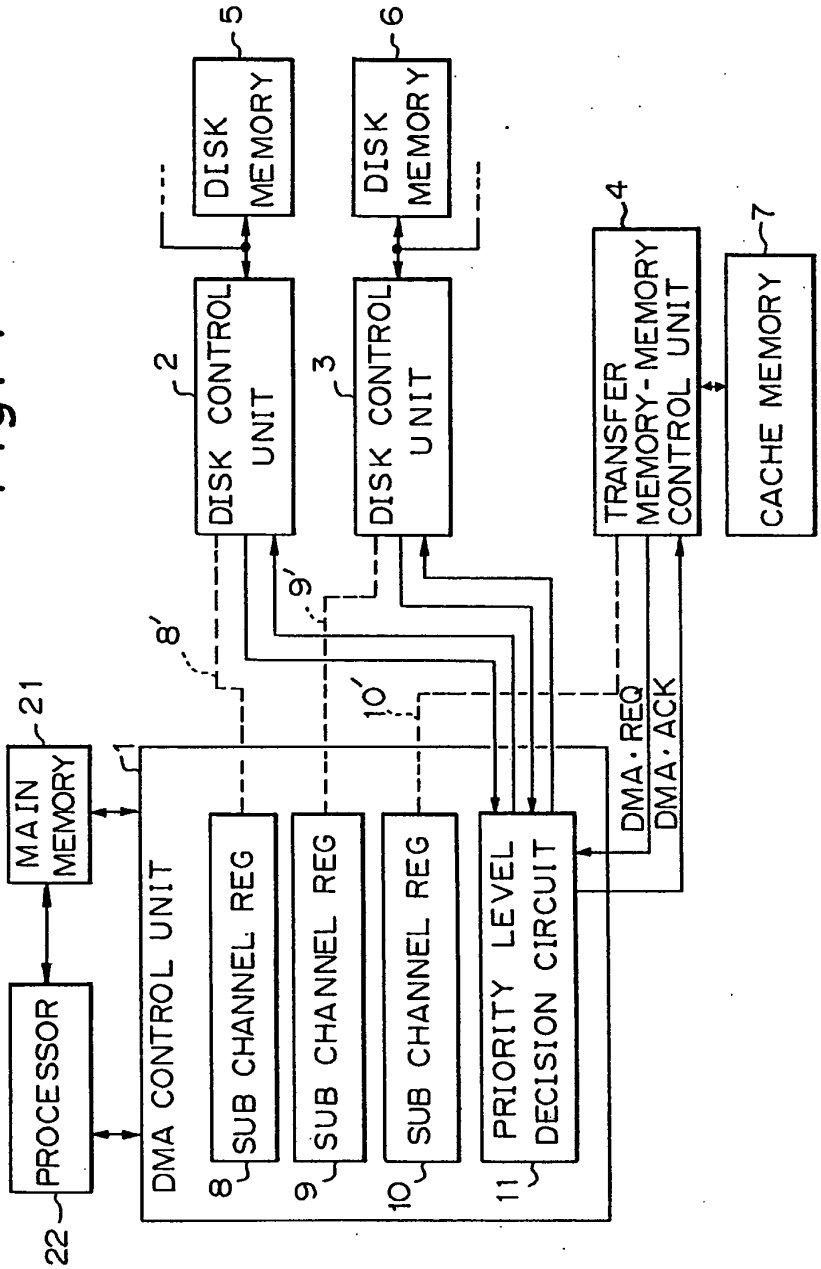

DISK MEMORY
5
DISK MEMORY
6
DISK CONTROL UNIT
2
DISK CONTROL UNIT
3
TRANSFER MEMORY-MEMORY CONTROL UNIT
4
CACHE MEMORY
7
8'
9'
10'
MAIN MEMORY
21
1
DMA CONTROL UNIT
SUB CHANNEL REG
8
SUB CHANNEL REG
9
SUB CHANNEL REG
10
PRIORITY LEVEL DECISION CIRCUIT
11
DMA·REQ
DMA·ACK
PROCESSOR
22

Fig. 2

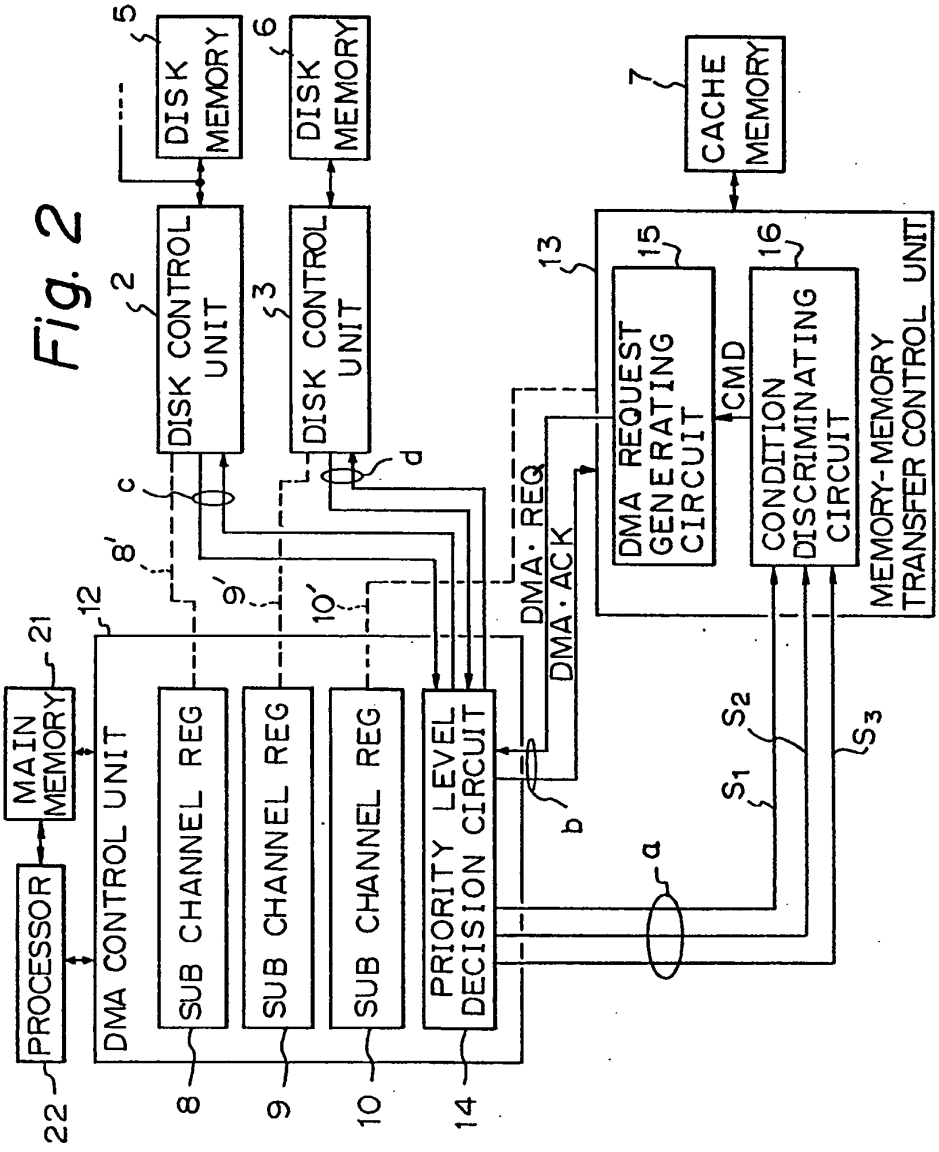

PROCESSOR
MAIN MEMORY
DMA CONTROL UNIT
SUB CHANNEL REG
SUB CHANNEL REG
SUB CHANNEL REG
PRIORITY LEVEL DECISION CIRCUIT
DISK CONTROL UNIT
DISK CONTROL UNIT
DISK MEMORY
DISK MEMORY
CACHE MEMORY
DMA REQUEST GENERATING CIRCUIT
CONDITION DISCRIMINATING CIRCUIT
MEMORY-MEMORY TRANSFER CONTROL UNIT
DMA·REQ
DMA·ACK
CMD
a
b
c
d
S1
S2
S3
8
9
10
14
22
12
21
2
3
5
6
7
13
15
16
8'
9'
10'

Fig. 3

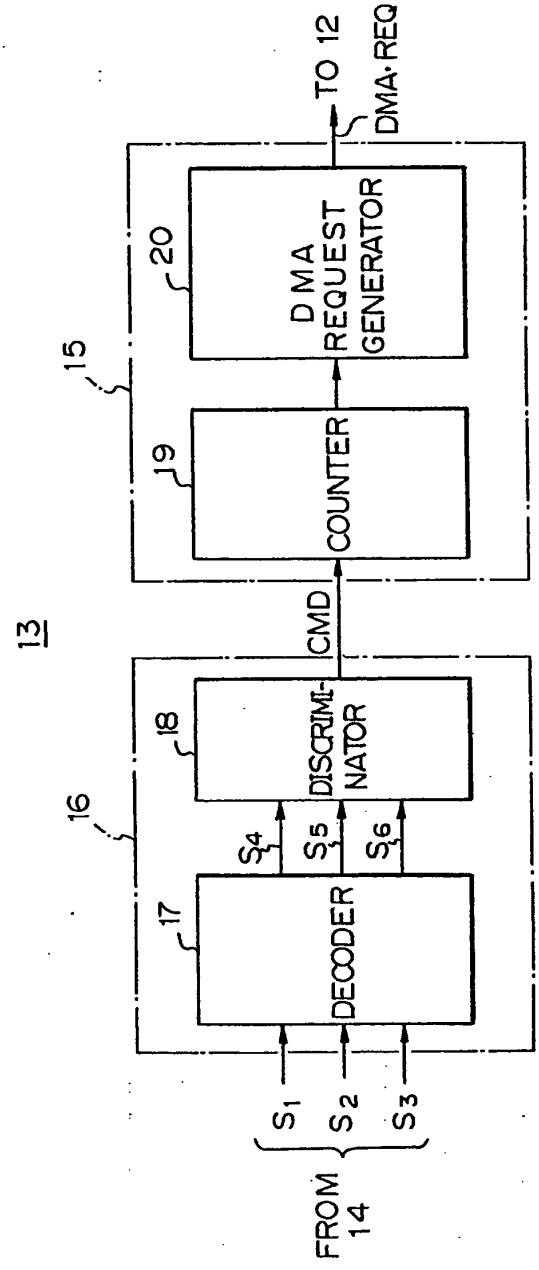
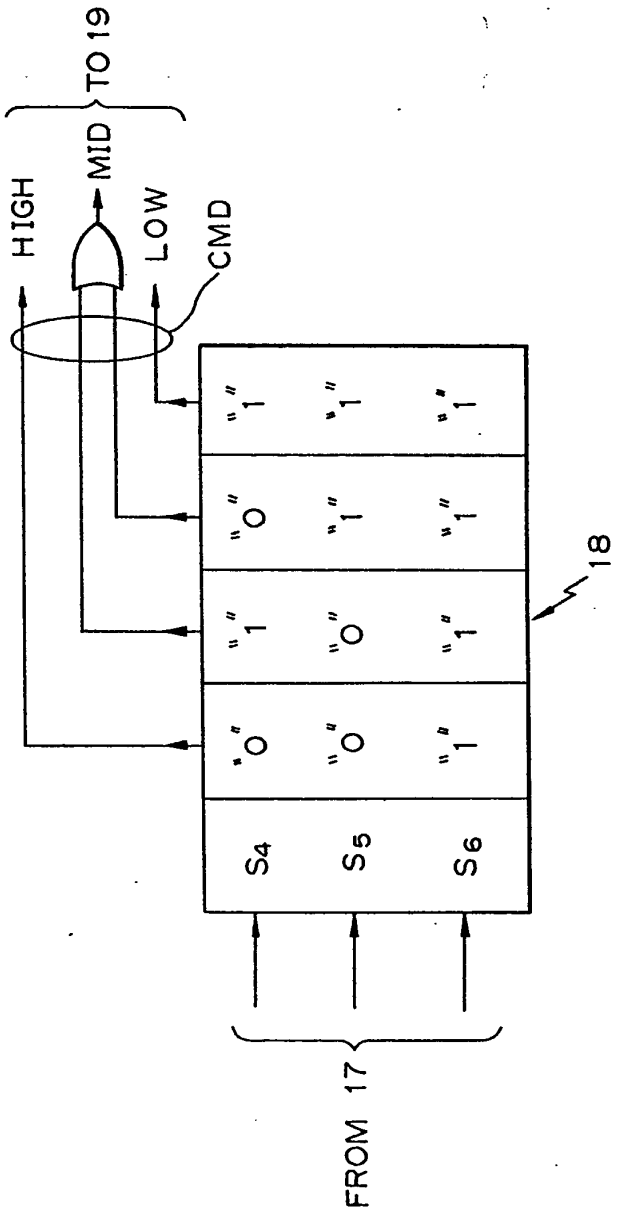

13
FROM 14
S1
S2
S3
16
17
DECODER
S4
S5
S6
18
DISCRIMI-NATOR
CMD
15
19
COUNTER
20
DMA REQUEST GENERATOR
TO 12
DMA-REQ

Fig. 4



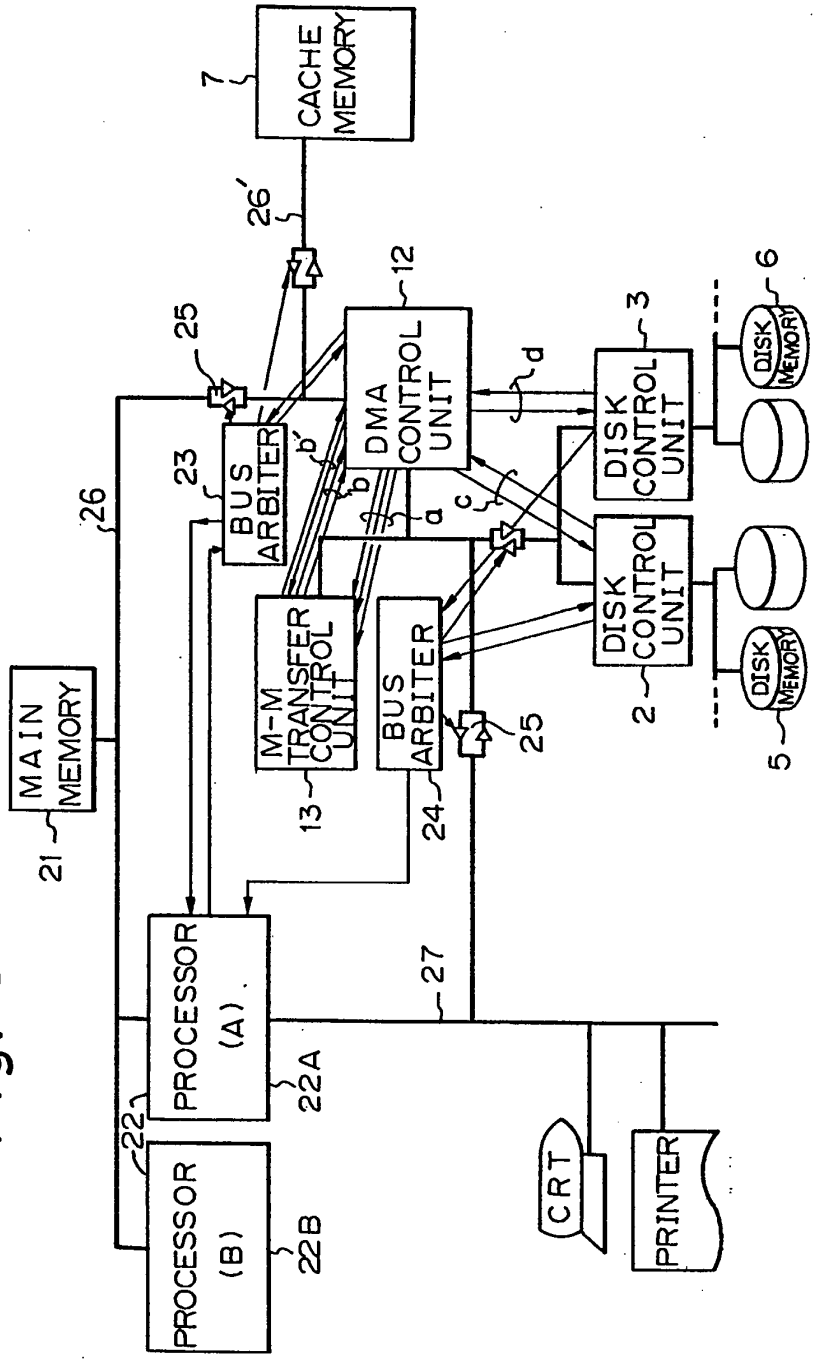

CACHE MEMORY
7
26'
25
12
DMA CONTROL UNIT
BUS ARBITER
23
26
M-M TRANSFER CONTROL UNIT
13
BUS ARBITER
24
25
MAIN MEMORY
21
PROCESSOR (A)
22A
PROCESSOR (B)
22B
27
DISK CONTROL UNIT
3
DISK CONTROL UNIT
2
DISK MEMORY
6
DISK MEMORY
5
CRT
PRINTER
a
b
b'
c
d

Fig. 5

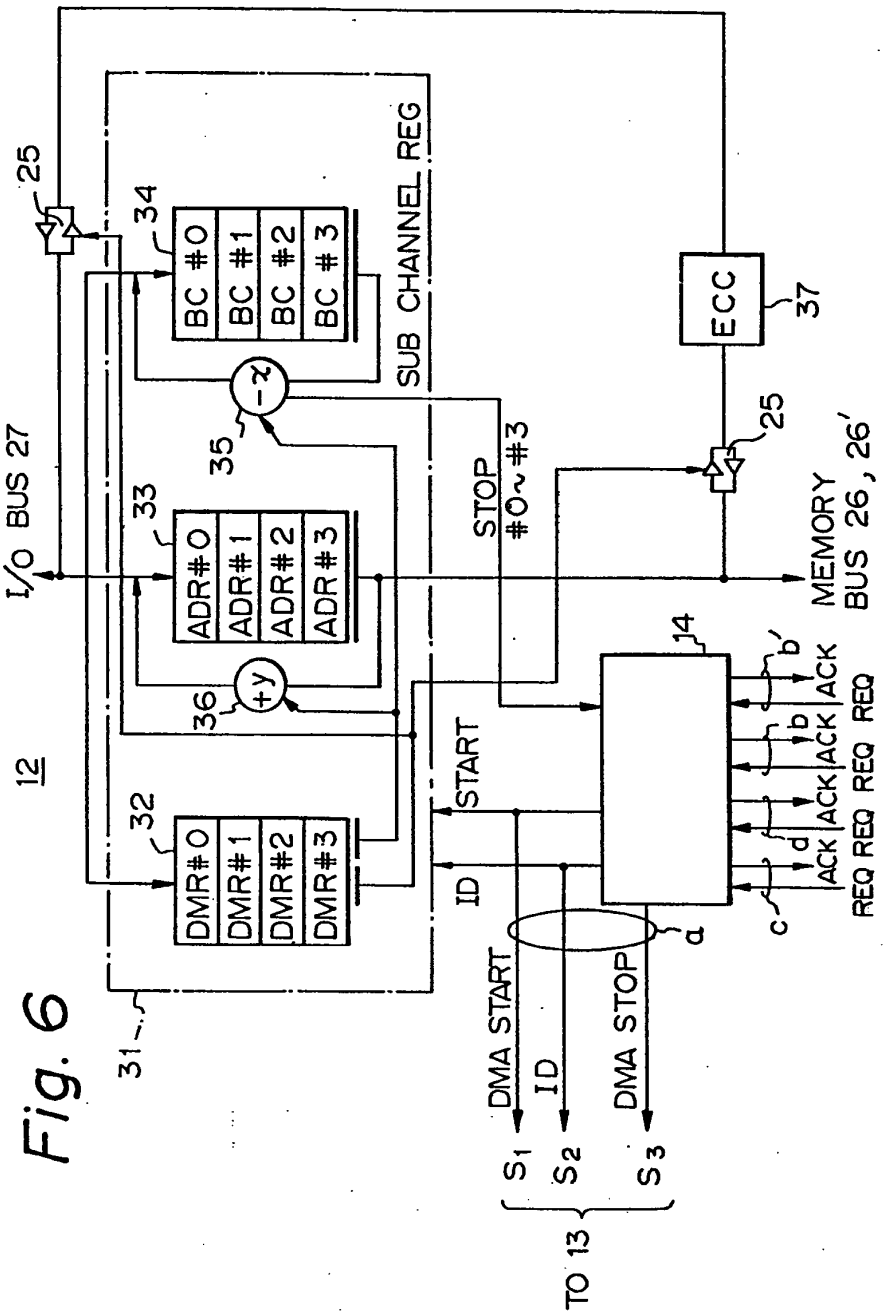

12
I/O BUS 27
25
34
BC #0
BC #1
BC #2
BC #3
SUB CHANNEL REG
35
-z
33
ADR#0
ADR#1
ADR#2
ADR#3
36
+y
32
DMR#0
DMR#1
DMR#2
DMR#3
31
START
ID
STOP #0~#3
ECC
37
25
MEMORY BUS 26, 26'
14
b'
b
d
c
a
ACK
REQ
DMA START
ID
DMA STOP
S1
S2
S3
TO 13

Fig. 6

Fig. 7

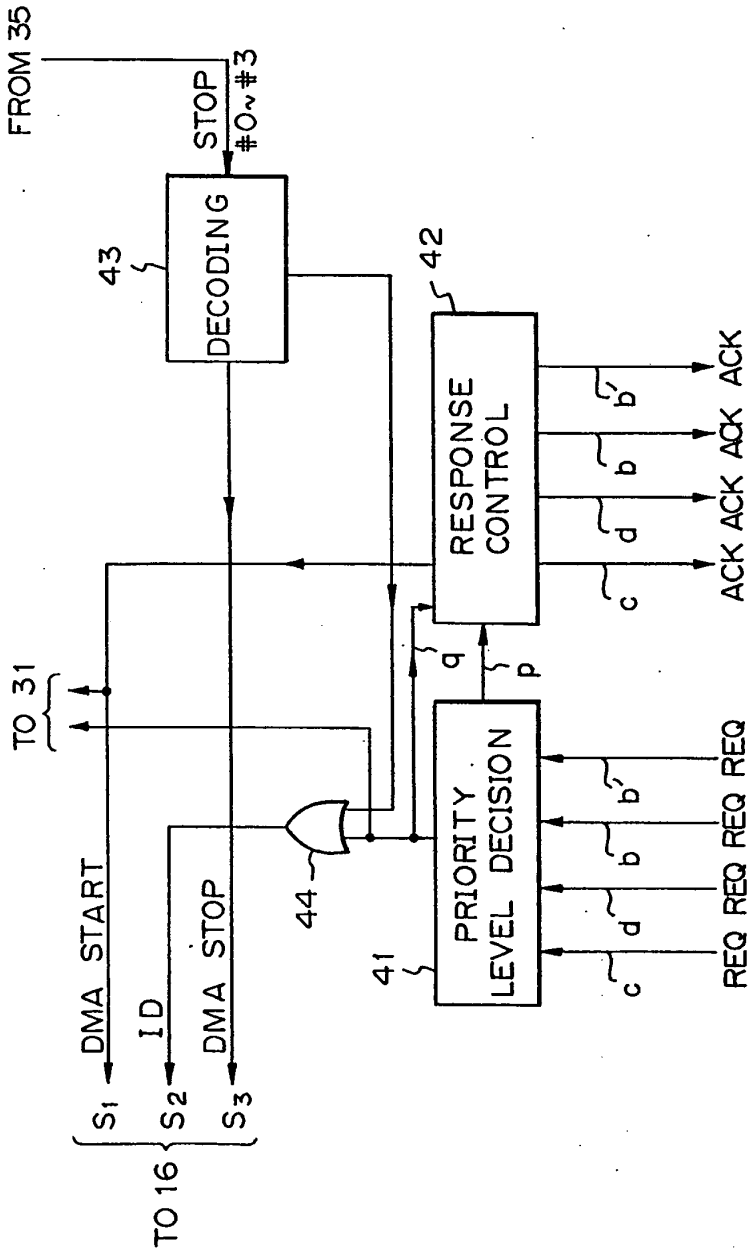

14
FROM 35
STOP
#0~#3
43
DECODING
42
RESPONSE CONTROL
ACK ACK ACK ACK
b' b d c
TO 31
q
p
PRIORITY LEVEL DECISION
41
REQ REQ REQ REQ
b' b d c
44
DMA START
ID
DMA STOP
S1 S2 S3
TO 16

Fig. 8

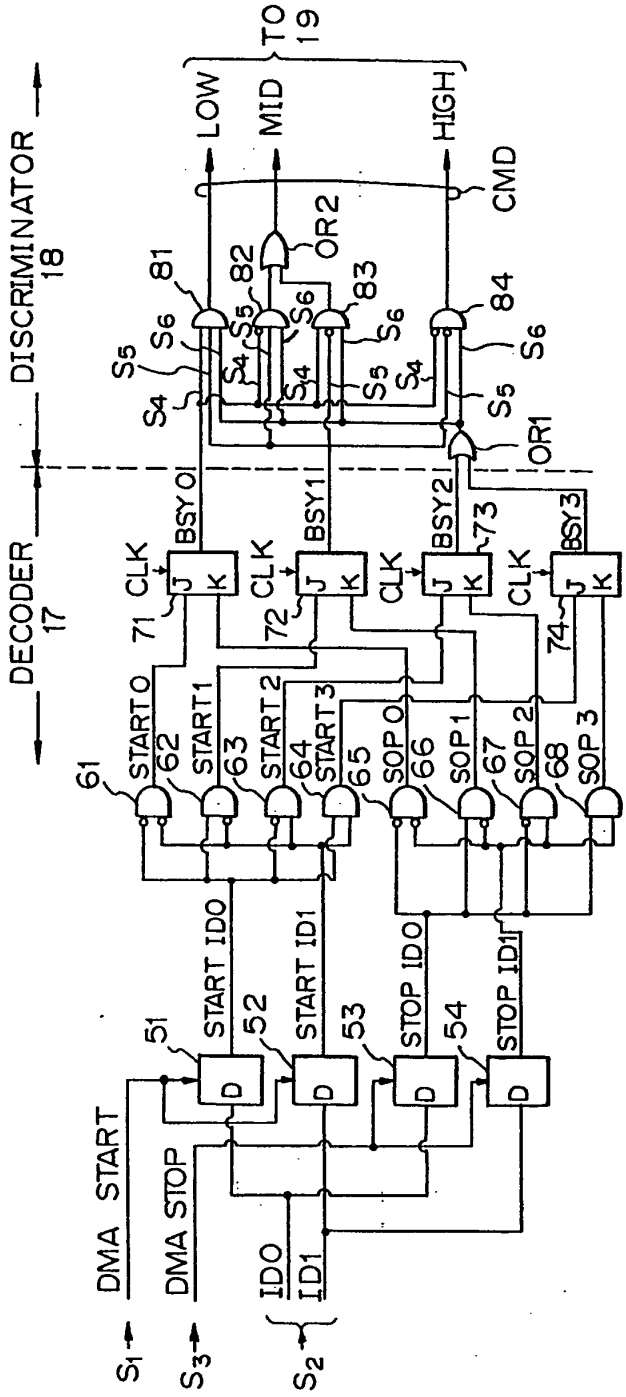
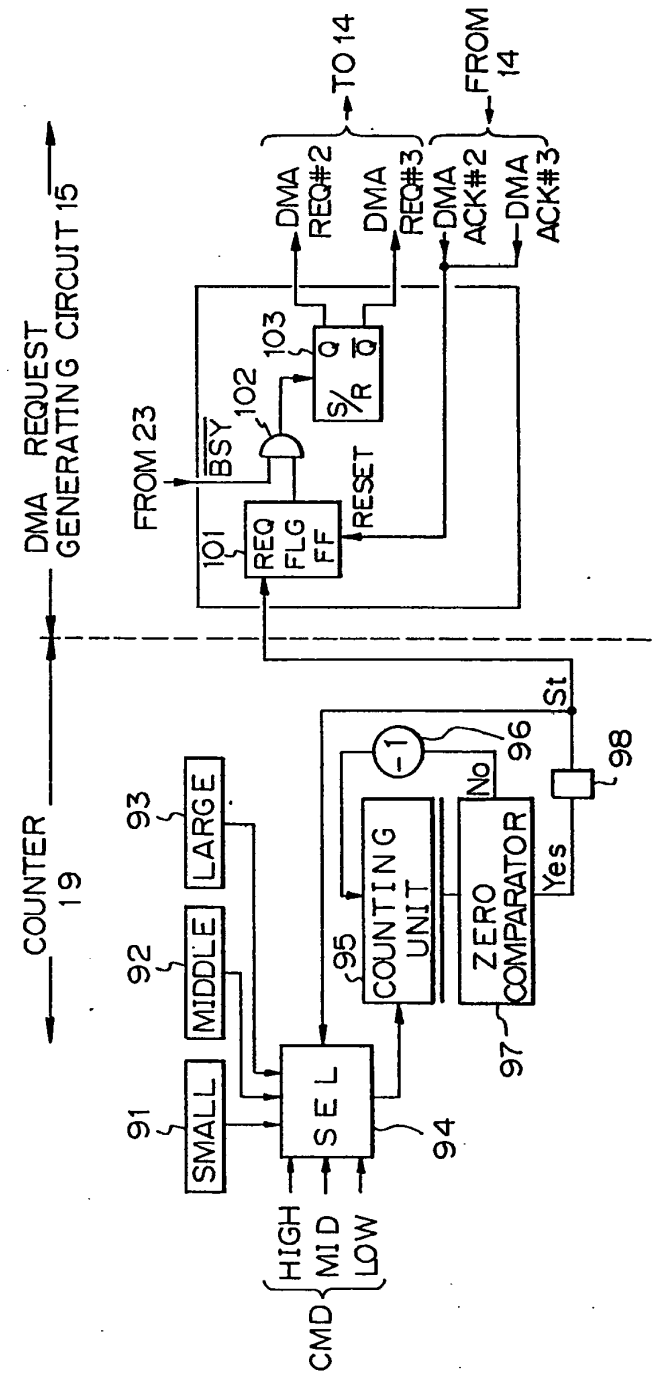

13
DECODER 17
DISCRIMINATOR 18
TO 19
LOW
MID
HIGH
CMD
OR1
OR2
BSY0
BSY1
BSY2
BSY3
CLK
J
K
D
START0
START1
START2
START3
SOP0
SOP1
SOP2
SOP3
START ID0
START ID1
STOP ID0
STOP ID1
DMA START
DMA STOP
ID0
ID1
S1
S2
S3
S4
S5
S6
51
52
53
54
61
62
63
64
65
66
67
68
71
72
73
74
81
82
83
84

Fig. 9


15
DMA REQUEST GENERATING CIRCUIT 15
COUNTER 19
FROM 23
BSY
102
101
REQ FLG FF
RESET
103
Q
S/R
Q̄
DMA REQ#2
DMA REQ#3
TO 14
FROM 14
DMA ACK#2
DMA ACK#3
93
LARGE
92
MIDDLE
91
SMALL
SEL
94
HIGH
MID
LOW
CMD
95
COUNTING UNIT
-1
96
No
Yes
ZERO COMPARATOR
97
St
98

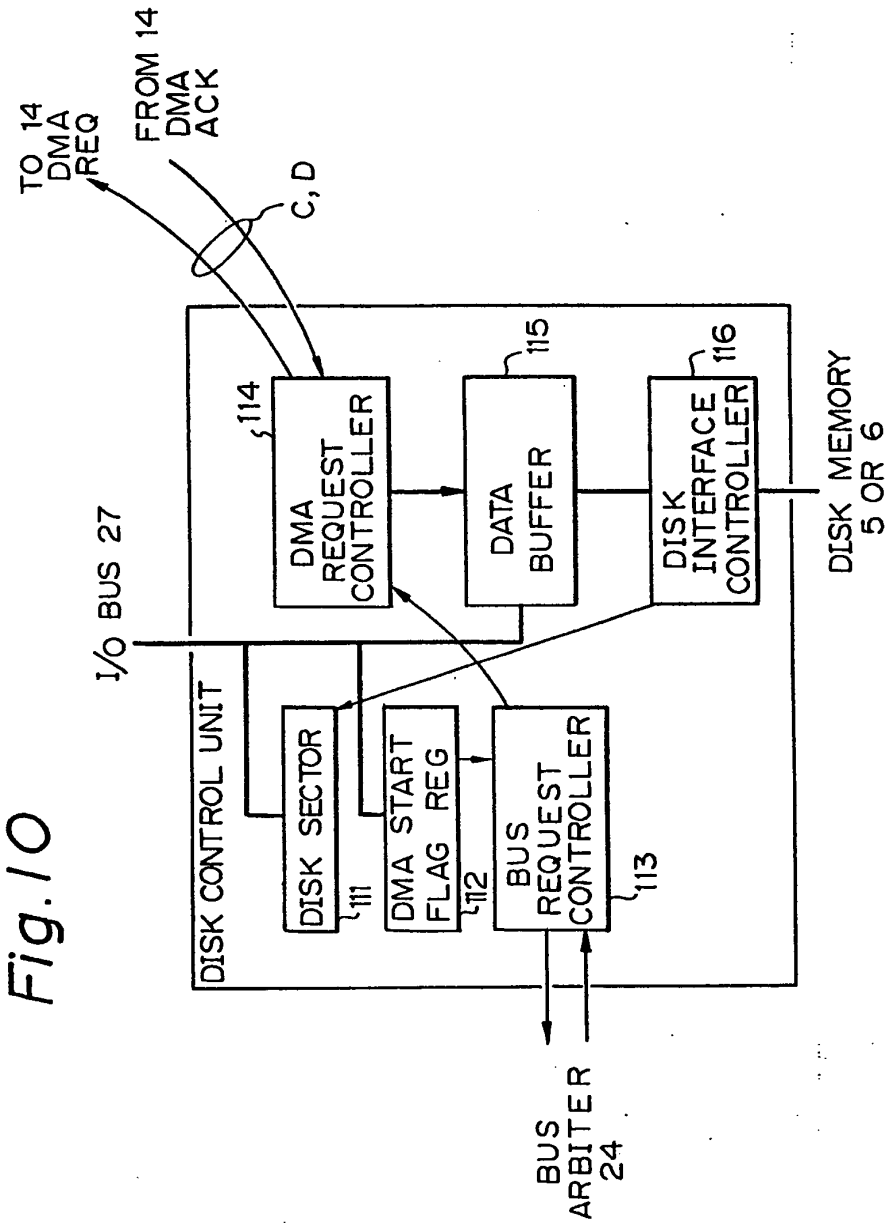

TO 14
DMA
REQ
FROM 14
DMA
ACK
C, D
I/O BUS 27
DISK CONTROL UNIT
DMA
REQUEST
CONTROLLER
114
DATA
BUFFER
115
DISK
INTERFACE
CONTROLLER
116
DISK MEMORY
5 OR 6
DISK SECTOR
111
DMA START
FLAG REG
112
BUS
REQUEST
CONTROLLER
113
BUS
ARBITER
24

Fig. 10